Improved Heat Sinking for Laser-Diode Arrays Using Microchannels in CVD Diamond

Kenneth E. Goodson, *Associate Member, IEEE*, Katsuo Kurabayashi, and R. Fabian W. Pease

***Abstract*— This work proposes a novel cooling system for high-power laser-diode arrays, for which the maximum optical output power density per unit surface area is limited by the temperature rise due to self-heating. The proposed system uses a microchannel heat sink made of chemical-vapor-deposited (CVD) diamond, whose high thermal conductivity increases the efficiency of the channel-wall fins and reduces the array-to-coolant thermal resistance using a simple model for the combined conduction and convection problem. The resistance is calculated to be 75% less than that for a conventional configuration using a silicon microchannel heat sink. The present analysis strongly motivates a future experimental study.**

***Index Terms*—Chemical-vapor-deposited (CVD) diamond, continuous wave (CW) laser-diode array, epitaxial lift-off, maximum output-power density, microchannel cooling, thermal resistance.**

I. Introduction

THE continuous wave (CW) operation of semiconductor laser-diode arrays benefits from a low thermal resistance for heat transfer from active regions to the environment. The maximum optical output power of these devices per unit surface area is limited primarily by the temperature rise at the diode junction due to self-heating [1], [2]. The temperature rise for a given self-heating power is proportional to the array-to-coolant thermal resistance. Three technologies, with varying levels of maturity, can be used to reduce the array-to-coolant thermal resistance.

1) One approach is to sandwich diamond films between the semiconducting substrate and the heat sink to improve lateral spreading of heat from the active regions [3], [4]. Sakamoto *et al*. [5] increased the total CW output power from 76–120 W by embedding a diamond submount between a AlGaAs/GaAs laser-diode array and a copper heat spreader.
2) Another approach to reducing the thermal resistance is to use convection in microchannels [6], which in the past have been etched into silicon. Missaggia *et al*. [7] mounted GaInAsP/InP buried heterostructure laser-diode arrays on a silicon microchannel heat sink using a solder joint, as depicted in Fig. 1, and measured the array-to-coolant thermal resistance using the temperature dependence of the threshold current density.
3) A third approach reduces the thickness of the semiconducting substrate between active regions and the heat sink using epitaxial lift-off (ELO) and grafting, which yield epitaxial GaAs films of thickness as thin as 200 Å on diamond substrates [8]. The back side of the very thin semiconducting substrate can be biased using metallic interfacial layers, such as those developed by Ersen *et al*. [9] for achieving atomically perfect grafting of GaAs to silicon. Because the thermal conductivities of GaAs and InP are more than one order of magnitude less than that of diamond, the close proximity of the diamond to active regions can strongly improve cooling. Until now, ELO and grafting have been used primarily to bring laser diodes in close contact with optically transparent substrates. Yablonovitch *et al*. [10] and Pollentier *et al*. [11] used ELO to fabricate a GaAs based laser diode on a glass or silicon substrate. Schumacher *et al*. [12] and Yi-Yan *et al*. [13] grafted an InP based semiconductor photo-device onto a glass or sapphire substrate.

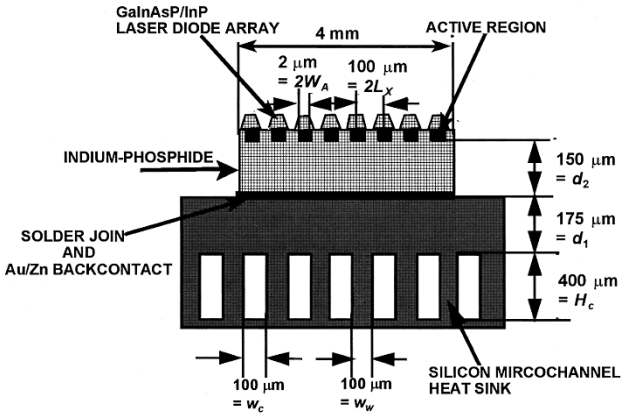

Fig. 1. Cross section of the silicon microchannel cooling system for GaInAsP/InP buried heterostructure laser-diode arrays developed by Missaggia *et al.* [7].

This work proposes a completely novel cooling system that combines all three technologies in the geometry shown in Fig. 2, which is expected to yield a lower bound for the array-to-coolant thermal resistance from laser-diode arrays. The new system uses microchannels within the diamond rather than within silicon. This eliminates the impact of the thermal boundary resistance at the diamond bottom boundary and uses the high conductivity of diamond to maximize the efficiency of the microchannel-wall fins. This work develops a simple model to compare the array-to-coolant thermal resistance for the novel system shown in Fig. 2 to the conventional system using a silicon microchannel heat sink shown in Fig. 1. The analysis employs an analytical solution to the steady-state,

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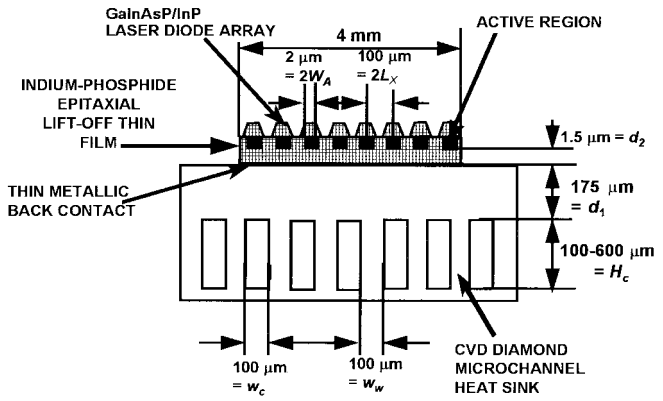

Fig. 2. Cross section of the microchannel cooling system proposed here for comparison with that of Missaggia *et al*. [7]. The new system for GaInAsP/InP buried heterostructure laser-diode arrays uses CVD diamond film for the heat sink.

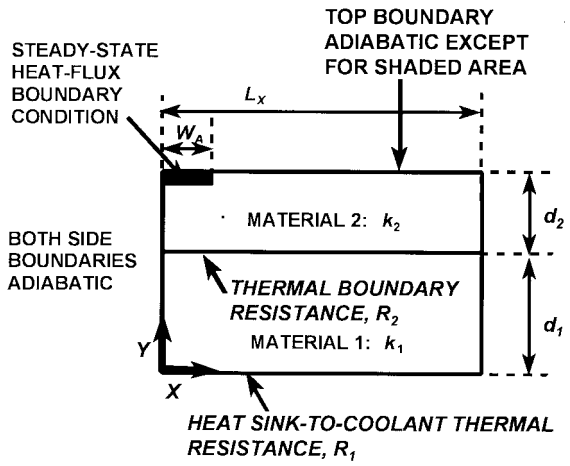

Fig. 3. Geometry used for the thermal-conduction analysis.

two-dimensional (2-D) thermal conduction equation and the bulk thermal properties of the constituent materials.

This work demonstrates the large potential improvement in the cooling of laser-diode arrays that can result from the use of microchannels in diamond, ELO, and grafting. This manuscript also describes previous research which makes the proposed laser-diode array structure feasible. The fabrication of this device is a major challenge for future work. The calculations provided here motivate this work.

II. Thermal Analysis

The array-to-coolant thermal resistance, R_{TOT}, is defined as the temperature rise at the center of an active stripe divided by the power per unit *total* surface area. For both configurations in Figs. 1 and 2, the calculation is performed for a 1 mm $\times$ 4 mm InP laser-diode array attached to the center of a microchannel heat sink with lateral dimensions of 1 cm$\times$1 cm.

The thermal resistance for an InP laser diode array on a silicon microchannel heat sink with these dimensions was measured by Missaggia *et al*. [7]. The laser diodes were arranged in a 2-D array with spatial periods of 250 μm and 100 μm. We simplified the geometry by assuming that the active-region length is equal to the spatial period in the direction with the 250 μm spatial period. This allows the active regions to be modeled as a one-dimensional (1-D) array of stripes with a center-to-center spacing of 100 μm.

Fig. 3 shows the geometry used for the thermal-conduction analysis. The active region is modeled using a uniform steady-state heat flux within a small region at the semiconductor substrate surface. This is a very rough approximation of the actual heat-source distribution in a laser-diode, which has been discussed, for example by Chen [14]. All surface except the active region is assumed to be adiabatic, which neglects radiation and convection from the diode array surface. The sides of the block are treated as adiabatic due to symmetry. In Fig. 4, d_1 is the thickness of the unchannelled heat sink substrate, d_2 is the thickness of the InP layer, $2L_X$ is the distance between the centers of the adjacent active stripes, and $2W_A$ is the active stripe width. The temperature dependence

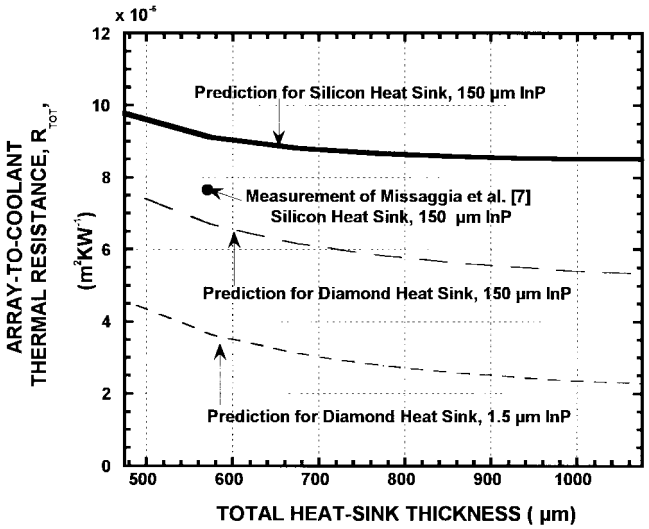

Fig. 4. Impact of the use of CVD diamond microchannels and grafted thin InP epitaxial lift-off films on the heat conduction in the microchannel cooling system for InP based laser-diode arrays.

and any nonhomogeneities of the thermal conductivities of the materials are neglected. Goodson *et al*. [15] discussed the importance of these approximations for a similar composite diamond-silicon substrate. The error in the thermal resistance is expected to be less than 20% for temperature rises less than 100 K. The dimensions and the thermal properties used for the thermal-conduction analysis are listed in Table I. It is assumed that the microchannels are fabricated in the CVD diamond film leaving 175-μm thick unchannelled region in the diamond substrate. The microchannels are oriented parallel to the active region stripes, as in the structure of Missaggia *et al*. [7].

In the configurations shown in Figs. 1 and 2, R_1 is the thermal resistance from the bottom of the unchannelled portion of the heat sink, made either of silicon or diamond, to the water coolant. If the water coolant flow rate is sufficiently large for given values of he microchannel width, w_c, and wall width, w_w, the coolant temperature rise can be neglected. This was demonstrated by the experiments of Missaggia *et al*. [7]

TABLE I
PARAMETERS USED IN THE THERMAL-CONDUCTION ANALYSIS. (a) CONVENTIONAL SYSTEM. (b) NOVEL SYSTEM PROPOSED HERE

Parameter in the Conventional Configuration shown in Fig. 1	Value
unchannelled silicon thickness, d_1	175 μm
InP substrate thickness, d_2	150 μm
lateral dimension of analyzed volume, $2L_X$	100 μm
active region width $2W_A$	2 μm
silicon thermal conductivity, k_1	150 W m^{-1} K^{-1}
InP thermal conductivity, k_2	70 W m^{-1} K^{-}

(a)

Parameter in the New Configuration shown in Fig. 2	Value
unchannelled diamond thickness, d_1	175 μm
InP substrate thickness, d_2	1.5 μm
lateral dimension of analyzed volume, $2L_X$	100 μm
active region width $2W_A$	2 μm
diamond thermal conductivity, k_1	2000 W m^{-1} K^{-1}
InP thermal conductivity, k_2	70 W m^{-1} K^{-}

(b)

for a flow rate of 2×10^{-5} m^{3}s^{-1} and $w_c = w_w$ =100 μm. The thermal resistance R_1 is therefore governed by convection from the microchannel walls, and is approximately given by [16]

$$R_1 = \left(\frac{D}{k_f \bar{\mathrm{N}}_u}\right)\left(\frac{w_c + w_w}{w_c + 2H_c\eta}\right). \tag{1}$$

The channel height is H_c, k_f is the thermal conductivity of water, and $\bar{\mathrm{N}}_u$ is the average Nusselt number for convection in the microchannels based on hydraulic diameter

$$D = \frac{2H_c w_c}{w_c + H_c}. \tag{2}$$

The microchannel-wall fin efficiency is

$$\eta = \frac{\tanh(N)}{N} \tag{3}$$

where

$$N = H_c\left(\frac{2k_f \bar{\mathrm{N}}_u}{k_w w_w D}\right)^{0.5} \tag{4}$$

where k_w is the thermal conductivity of the material used for the microchannel heat sink. For the conventional configuration in Fig. 1, k_w is the thermal conductivity of silicon. For the new configuration in Fig. 2, k_w is the thermal conductivity of diamond. For an infinite microchannel depth H_c and the same values of w_c and w_w, the fin efficiency η for the diamond microchannel is 3.6 times larger than that for the silicon microchannel due to the difference in the thermal conductivites. Therefore, R_1 is reduced through the use of diamond. The present analysis uses $w_c = w_w$ =100 μm, and a pressure drop along the microchannels of Δp =482 kPa, as in the experiments of Misaggia *et al.* [7]. The Reynolds number based on the hydraulic diameter is

$$\mathrm{Re}^2 = \frac{\rho D^3 \Delta p}{2 f_{app} \mu^2 L} \tag{5}$$

where ρ and μ are the density and dynamic viscosity of water, respectively. The microchannel length is L, and f_{app} is the apparent friction factor along the entire channel. The Reynolds number is calculated using (5) and a correlation for turbulent flow relating f_{app}, Re, and L/D [16]. The values of Re are greater than 2300, the critical Reynolds number of internal flow, confirming that the flow is turbulent. The average Nusselt number, $\bar{\mathrm{N}}_u$, is calculated by integrating the correlation for the local Nusselt number along the channel in the turbulent regime [16], [17]. For example, if $w_c = w_w = 100$ μm, $H_c = 400$ μm, and $L = 1$ cm, then (2) yields $D = 160$ μm and Re is approximately 2750 from (5). The average Nusselt number is approximately $\bar{\mathrm{N}}_u = 20$. Equations (1)–(3) yield $R_1 = 3.8 \times 10^{-6}$ m^2·KW^{-1} for the silicon microchannel heat sink and $R_1 = 2.7 \times 10^{-6}$ m^2·KW^{-1} for the diamond microchannel heat sink.

For the conventional configuration shown in Fig. 1, R_2, models the effective InP-Si thermal boundary resistance and is governed by thermal conduction normal to the solder joint. The solder is assumed to have the thickness $d_s = 10$ μm and thermal conductivity $k_s \approx 40$ Wm^{-1}K^{-1} [18], yielding the boundary resistance $R_2 = d_s/k_s = 2.5 \times 10^{-7}$ m^{2}KW^{-1} This is a lower bound for the boundary resistance because it does not account for porosity in the solder. In the new configuration, R_2 is the thermal resistance at the InP-diamond boundary. This boundary consists of a thin metallic layer for biasing the metallic interfacial layers, Ersen *et al.*, [9] achieved atomic-scale perfection for GaAs-silicon interfaces using Pd and Cr interfacial layers. It is assumed here that similar facilitating metal interfacial layers can be developed for the InP-diamond interfaces in the present study. The thermal resistance of such an interface would be very small compared to the volume thermal resistance in the semiconductor, and is therefore neglected here.

The maximum temperate rise in the active region is determined by solving the heat-conduction equation in closed form using the method of Fourier series. The ratio of the temperature rise to the power dissipated per unit total surface area is the array-to-coolant thermal resistance (6) as shown at the bottom of the next page, where the parameters λ_n and S_n are

$$\lambda_n = \frac{n\pi}{L_X} \tag{7}$$

$$S_n = \begin{cases} 1 & (n = 0) \\ \frac{2L_X}{n\pi W_A}\sin(\lambda_n W_A) & (n \geq 1). \end{cases} \tag{8}$$

III. RESULTS AND DISCUSSION

For the case of the conventional geometry of Missaggia *et al.* [7], the present work calculates an array-to-coolant thermal resistance of 9.1×10^{-6} m^2·KW^{-1}. This agrees fairly well with the value measured by those authors, 7.9×10^{-6} m^2·KW^{-1}.

Fig. 4 compares the array-to-coolant thermal resistance as a function of the total heat sink thickness for the cases of

the novel structure using diamond microchannels and the conventional structure using silicon microchannels. The relatively high cost of fabricating a diamond layer increases with its thickness. The array-to-coolant thermal resistance decreases with increasing values of the microchannel height due to the increasing area for convection. The high-conductivity diamond helps maintain a relatively-high fin efficiency as the height is increased. The data point in the curve shown in Fig. 5 is the array-to-coolant thermal resistance for the conventional configuration with the dimensions used by Missaggia *et al*. [7], i.e., $w_c = w_w = 100\ \mu$m, $H_c = 400\ \mu$m, 175 μm unchannelled silicon substrate, and 150 μm InP substrate.

For the diamond microchannels of 900 μm height, the plot in Fig. 5 predicts a 35% reduction in the array-to-coolant thermal resistance for the arrays having the 150 μm InP substrate with respect to the conventional configuration given by Missaggia *et al*. [7]. If the laser-diode arrays are assumed to be fabricated using ELO/grafting technology as shown in Fig. 2, a 75% reduction in the array-to-coolant thermal resistance can be obtained compared to that for the conventional configuration for the same channel height as above. This indicates that the maximum output power density of the laser diode array, which is limited by the resulting temperature rise, can be increased from 10^7 Wm^{-2}, which is obtained in the conventional configuration, to 4×10^7 Wm^{-2} with the given microchannel geometry. For the geometry considered here, the combination of diamond microchannel heat sink technology and ELO/grafting technology has a much larger effect on the thermal resistance reduction than the use of the diamond microchannel technology alone.

IV. Future Experimental Work

The thermal analysis performed here predicts that the proposed diamond microchannel cooling system yields remarkable heat sinking improvement for the high-power laser-diode arrays compared to the cooling system fabricated using the conventional silicon etching technique. The use of diamond microchannels and ELO/grafting technology, both of which remain relatively immature, will bring challenges in cost-effectiveness, reliability, and manufacturability.

A high growth rate of CVD diamond is essential for achieving low-cost fabrication of the diamond cooling system. Recent work using an RF plasma torch reports a deposition rate approaching 50 μmh^{-1} [19]. This means that the growth rate is currently more than three orders of magnitude larger than those achieved in early 1980s. Singer [20] estimates the cost will be reduced within the next five to ten years to about ten dollars per chip carrier of dimension $1.0\times1.0\times0.1$ cm^3, which is approximately one tenth of the current cost. This assessment assumes that the cost reduction resulting from a higher deposition rate can be achieved through further optimization of reactor settings. Continuous increase of deposition rate and area coverage due to the technological improvement may provide a low-cost high-volume diamond growth process required for the proposed cooling system in the future.

Selective seeding and deposition of CVD diamond are promising techniques for patterning diamond microstructures on silicon substrates [21], [22]. Photoresist patterns are fabricated by conventional lithography using photoresist mixed with fine diamond powder. The photoresist patterns serve as nucleation/growth sites on the substrate during the deposition process and the same patterns of diamond are formed on the substrate. A fabrication of diamond bridges as narrow as 1 μm width has been achieved using this method [22]. A similar approach may be taken to fabricate the diamond microchannels. But it must be noted that the high aspect-ratio microchannel feature might yield a technical challenge to be overcome in the fabrication process.

The CVD diamond growth process results in faceted surface morphology which must be polished before it can be appropriate for ELO and grafting. A relatively fast and cost-effective surface polishing technique is needed to yield the high-quality interface between the ELO film and the diamond heat sink. Jin *et al*. [23] developed a polishing technique of CVD diamond using a chemical reaction of manganese powder with diamond. A SEM image shows that a CVD diamond surface with rough facets of 20–60 μm variation in height is optically smooth after a 5 min HCl etching process subsequent to 48 h annealing of the sample. The large reactivity of manganese with diamond reduces the etching time and may contribute to fabrication cost reduction.

The device performance of the InP laser-diode arrays in the cooling system described here depends on the film quality resulting from the ELO and grafting process as well as effective heat conduction. Yablonovitch *et al*. [24] used thermal cycling to demonstrate reliable bonding of ELO GaAs films to a silicon substrate. Other studies [13], [25], [26] show that the ELO process causes no significant change in film properties, such as carrier density, carrier mobility, and optical quality, before and after the lift-off. Dingle *et al*. [27] integrated a prototype GaAs-based LED array on a silicon substrate using the ELO technology and obtained 75 percent yield out of 90 separate functioning LED's in the array. Process automation may be possible due to the simplicity of the ELO and grafting technology, which should increase the device yield and lead to the cost reduction.

$$R_{TOT} = \sum_{n=0}^{\infty}\left[\frac{S_n\left[k_1(R_1+R_2)\lambda_n + \left(1+k_1^2R_1R_2\lambda_n^2\right)\tanh(\lambda_n d_1) + \frac{k_1}{k_2}\tanh(\lambda_n d_2) + \frac{k_1}{k_2}R_1\lambda_n\tanh(\lambda_n d_1)\tanh(\lambda_n d_2)\right]}{\lambda_n\left[k_1 + k_1^2R_1\lambda_n\tanh(\lambda_n d_1) + k_1k_2(R_1+R_2)\lambda_n\tanh(\lambda_n d_2) + k_2\left(1+k_1^2R_1R_2\lambda_n^2\right)\tanh(\lambda_n d_1)\tanh(\lambda_n d_2)\right]}\right] \tag{6}$$

The microchannel cooling technology implemented at laboratory generally requires a water supply/drain system to provide the coolant flow through the heat sink channels and a pressure regulator to control the coolant pressure drop across these channels. This will increase the cost of implementation of the technology for compact electronic component cooling, and will need to be weighed against the substantial improvement in cooling capability.

V. Conclusion

A new microchannel cooling system is proposed for laser-diode arrays incorporating CVD diamond microchannel technology and epitaxial lift-off (ELO) and grafting. The present analysis shows that this new configuration has the potential to yield a 75% reduction in the thermal resistance from the diode array to the water coolant compared to that for a conventional configuration based on microchannels in silicon. As a result, the maximum output-power density per unit surface area of the laser-diode arrays can be increased by a factor of four. This reduction in the thermal resistance results from the use of both novel technologies proposed here, i.e., microchannels in CVD diamond and ELO/grafting. The potential reduction for geometries other than that of Missaggia *et al*. [7], which is used for comparison here, can be much larger. The impact of using diamond rather than silicon for a given heat sink thickness increases with decreasing microchannel width. The benefit of using thin device substrates through ELO/grafting technology increases with increasing active layer width. The predictions calculated here provide the theoretical basis for further experimental work. The future experimental work needs to include several technological innovations that make the proposed cooling system ready for practical implementations.

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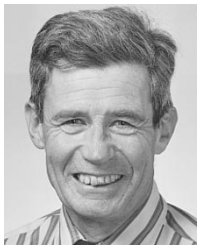

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After spending one year as a Research Fellow at Trinity College, Cambridge, he joined the faculty at the University of California, Berkeley, and continued research on scanning microscopy. In 1967, he joined Bell Telephone Laboratories where he first worked on the digital encoding of television signals and then on electron beam and X-ray lithography. During that time he supervised a group responsible for developing technology for using the Bell Laboratories electron beam exposure system EBES and sensitive electron beam resists for mask making and for direct write on the wafer. Since 1978, he has been a Professor of Electrical Engineering at Stanford University, Stanford, CA, and is conducting a research program into the generation and applications of microstructures. His projects include the generation and application of high resolution electron and ion beams, novel approaches to deep ultra-violet lithography, nonconventional resists, direct write technology, X-ray lithography, heat transfer in microstructures, and new approaches to interconnecting VLSI chips.